REMARKS

Applicant would like to thank Examiner Chang for the courtesy of an interview on May 28, 2008. Applicant presented arguments regarding the average voltage change being greater than 6 V/us in *Yamomoto et al.* (U.S. 5,142,200) and that a set-up pulse and a sustain pulse are functionally different. No agreement was reached regarding the allowability of the claims, however Examiner Chang agreed to consider the arguments submitted herein.

Claims 100–115 are newly added but do not add any new matter.

The Office Action rejected Claims 88-99 under 35 U.S.C. §112 as being indefinite. Applicant has amended Claim 88 to overcome the rejection.

The present invention is directed towards a plasma display panel utilizing a setup pulse with an average rise rate no greater than 6 V/us. This advantageously reduces the amount of accidental light emitted by the set-up pulse discharge such that it is much weaker than the light emitted by the sustain discharge. By doing so, contrast is also almost totally unaffected. (Pg. 28, Lns. 2–8)

The Office Action rejected Claims 51-99 under 35 U.S.C. §103 as being unpatentable over Applicant's Admitted Prior Art ("AAPA") in view of *Yamamoto*.

The Office Action admits that AAPA does not teach or suggest "a set-up step for applying a set-up pulse to each of the plurality of discharge cells to increase wall charges in the discharge cells, wherein the set-up pulse applied in the set-up step has a waveform that rises at an average voltage change rate of no greater than 6 V/μs, and that starts to fall at a rate greater than the average voltage change rate at a time period of the rising."

However, *Yamamoto* does not teach or suggest "a set-up step for applying a set-up pulse to each of the plurality of discharge cells to increase wall charges in the discharge cells, wherein

the set-up pulse applied in the set-up step has a waveform that rises at an average voltage change rate of no greater than 6 V/μs, and that starts to fall at a rate greater than the average voltage change rate at a time period of the rising."

Yamomoto does not teach that the set-up pulse is no greater than 6 V/μs and *Yamomoto* only teaches modifications to a sustain pulse instead of a set-up pulse. Furthermore as shown in Figure 5a of *Yamamoto*, the time for TA is between 150 ns to 500 ns, which is equivalent to 0.15 μs to 0.5 μs. (Col. 5, lns. 37–56) During time TA, the voltage of the sustain pulse rises 0.95 V_{SP} which is 142.5 V when V_{SP} is 150 V. (Col. 5, lns. 24–30; Col. 6, lns. 4–24). Thus, during time T_A, the rise rate of the sustain pulse ranges from 142.5 V / 0.5 μs, or 285 V/μs to 142.5 V/ 0.15μs which is 950 V/μs. This is vastly larger than the 6 V/μs average rise rate disclosed in the present invention for a set-up pulse.

Furthermore, even if hypothetically the rise rate is calculated based on the entire sustain pulse time period (T_A + T_P), and there is no indication that it should be so calculated in *Yamamoto*, the rise rate disclosed in *Yamomoto* would be 68.18 V/μs and would still be significantly larger than the rise rate disclosed in the present invention for a setup pulse. The maximum time T_P is 1.7 μs, thus the maximum time for TA + TP is 0.5 us + 1.7 μs, which is 2.2 μs. (Col. 6, lns. 49 -52) Over that time period, the maximum Voltage is V_{SP}, which is 150 V. Thus, the rise rate for T_A + T_P is 150 V/2.2 μs = 68.18 V/μs which is still vastly larger than the 6 V/μs average rise rate disclosed in the present invention for the set-up pulse.

> A particular parameter must first be recognized as a result-effective variable, i.e., a variable which achieves a recognized result, before the determination of the optimum or workable ranges of said variable might be characterized as routine experimentation. *In re Antonie*, 559 F.2d 618, 195 USPQ 6 (CCPA 1977) (The claimed wastewater treatment device had a tank volume to contractor area of 0.12 gal./sq. ft. The prior art did not recognize that treatment capacity is a function of the tank volume to

> contractor ratio, and therefore the parameter optimized was not recognized in the art to be a result-effective variable.).
>
> MPEP §2144.05 (II)(B) (underline added)

The Office Action also contended that it would have been obvious to a person of ordinary skill to use a voltage rise rate for a sustain pulse for a setup pulse and furthermore that it would have been obvious to use any rise rate. However, the smallest acceptable rise rate for sustain pulses is 20.8 V/μs in an AC Plasma Display Panel, which is larger than the 6 V/μs disclosed in the present invention.

As noted in MPEP §2144.03

> It would not be appropriate for the examiner to take official notice of facts without citing a prior art reference where the facts asserted to be well known are not capable of instant and unquestionable demonstration as being well-known... . If applicant adequately traverses the examiner's assertion of official notice, the examiner must provide documentary evidence in the next Office Action if the rejection is to be maintained.

As seen in Figure 3 of the present invention, each field which is a standard 1/60s long, or 16,700 μs, includes 8 sub-fields. Each sub-field is comprised of 1 setup period, 1 write period, and 1 discharge sustain period. Setup periods and write periods have constant amount of pulses and length in each sub-field while sustain periods vary by weighting based on the sub-field.

The shortest approximate acceptable length for a setup period within each sub-field is 150 μs. Thus, the minimum amount of time required for the setup period for the whole field is 8 x 150 μs = 1,200 μs. The shortest acceptable length for each write period is 1.0 μs. However, there are a minimum of 768 scanning lines. Assuming dual scan technology, and there is no indication that such technology should be used, there are a minimum of 768/2 = 384 scanning

lines that need to be scanned for each sub-field, with each scanning line taking 1.0 μs. Thus, the write period for the field is 8 x (768/2) x 1.0 μs = 3,072 μs, or approximately 3,000 μs.

Subtracting the time required for the write periods and setup periods from the time in the field yields the amount of time remaining for sustain pulses: 16,700 μs (time period of the Field) – 1,200 μs (setup pulses) – 3,000 μs (write pulses) = 12,500 μs (time remaining for sustain pulses).

Thus, there are 12,500 μs remaining in the field for the sustain pulses. Within each of the 8 sub-fields, the number of sustain pulses vary based on a weighting system where the first sub-field has a discharge sustain period weight of $2^0 = 1$, second sub-field has a discharge sustain period weight of $2^1 = 2$, and the eighth sub-field has a discharge sustain period weight of $2^7 = 128$ for a total of 255 sustain period weights for all 8 sub-fields. That is, the first sub-field has the minimum number of sustain pulses, the second sub-field has 2 times as many sub-fields as the number of sub-fields in the first sub-field, and the eighth sub-field has 128 times as many sustain pulses as the number of sustain pulses in the first sub-field. The minimum number of sustain pulses in the first sub-field in order for the first sub-field to perform adequately is 3. Furthermore, each sustain pulse must be applied to each scanning line and each sustain line. Thus, there are 255 x 3 x 2 sustain pulses in the field, which is 1530 sustain pulses. 12,500 μs / 1530 is approximately 8.17 μs for each sustain pulse. In an AC Plasma Display Panel in the present invention as opposed to a DC Plasma Display Panel disclosed in *Yamomoto*, the minimum acceptable voltage V_{SP} for a sustain pulse in AC Plasma Display Panels in order to maintain acceptable picture quality is170 V.

170 V / 8.17 μs is 20.8 V/μs, which is again much greater than the 6 V/μs average rise rate disclosed in the present invention for the set-up pulse. Even if the 150 V disclosed in

Yamamoto was used, the lowest acceptable sustain pulse rise rate would be 150 V / 8.17 μs = 18.36 V/μs, which is still much larger than the 6 V/μs average rise rate disclosed in the present invention for the set-up pulse.

In addition, the setup pulse is required to perform different functions than the sustain pulse as seen in the Attachment A hereto.

Attachment A is a schematic view of pulse functions within their respective time periods. As seen in Attachment A, during a set-up period, the set-up pulse accumulates wall charges between scan electrode 19a and the data electrode 14 by using a weak discharge to accelerate the write discharge in the write period. The weak discharge should minimize light emission to increase the contrast in the sustain period. During the write period, the write pulse causes a discharge between the scan electrode 19a and the data electrode 14 to accumulate positive wall charges on the scan electrode 19a in select discharge cells.

However, during the sustain period, the sustain pulse is alternately applied to the scan electrode 19a and the sustain electrode 19b to cause a discharge with a brightness required for image display. By alternately applying the sustain pulse to the scan electrode 19a and the sustain electrode 19b, the positive and negative charges alternate in accumulating between the scan electrode 19a and the sustain electrode 19b. This maintains the plasma in a sufficiently excited state and allows sufficient emission of ultraviolet rays to excite the phosphorous to provide the brightness required for image display. During the erase period, the erase pulse is applied to erase wall charges so as to not influence subsequent fields.

Thus, in the setup period, the setup pulse accumulates wall charges between scan electrodes 19a and data electrodes 14 by weak discharge. Accumulating wall charges allows a write discharge to occur more easily in the write period. This weak discharge effect should be

minimized to reduce any accidental discharge of light and to improve contrast during the sustain period. (Pg. 4, lns. 5–6).

However, in the sustain period, the sustain pulse is applied alternately to the scan electrodes 19a and the sustain electrodes 19b, thereby causing a discharge to occur in the select discharge cells. In contrast to the setup period, the discharge that occurs during the sustain period must be sufficient to obtain a brightness required for image display. (Pg. 4, lns. 11–15).

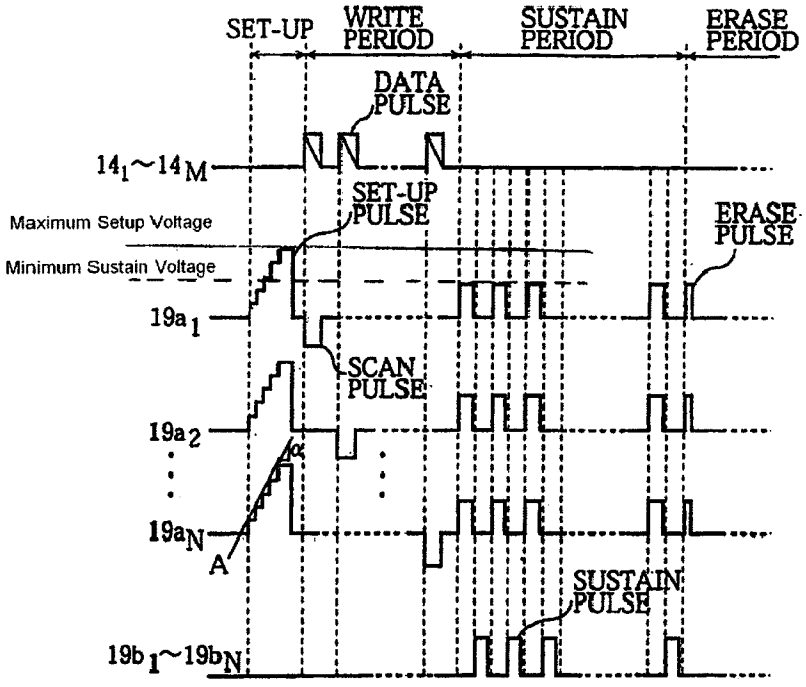
This is further evident by the discovery in the present invention where if the average rate of voltage change for a setup pulse is less than 6 V/μs, any light inadvertently emitted by the set-up pulse discharge is much weaker than the light emitted by the sustain discharge and contrast is almost totally unaffected. (Pg. 28, lns. 2–8). Thus, the setup pulse in the present invention is used to prevent deterioration of contrast, especially when compared with the discharge that occurs when the sustain pulse is used.

As noted in *Ex parte* Karoleen B. Alexander, No. 2007-2698, slip op. at 6 (B.P.A.I. Nov. 30, 2007):

> It is the Examiner's burden to establish *prima facie* obviousness. *See In re Rijckaert*, 9 F.3d 1531, 1532 (Fed. Cir. 1993) Obviousness requires a suggestion of all the elements in a claim *(CFMT, Inc. v. Yieldup Int'l Corp.*, 349 F.3d 1333, 1342 (Fed. Cir. 2003)) and "a reason that would have prompted a person of ordinary skill in the relevant field to combine the elements in the way the claimed new invention does." *KSR Int'l Co. v. Teleflex Inc.*, 127 S. Ct. 1727, 1741 (2007). Here, we find that the Examiner has not identified all the elements of claim 1, nor provided a reason that would have prompted the skilled worker to have arranged them in the manner necessary to reach the claimed invention.

As shown in Figure 15 of the present invention, the setup pulse and the sustain pulse also appear structurally different. In Figure 15 below, the magnitude of the voltage of the setup pulse is larger than the magnitude of the voltage of the sustain pulse:

FIG. 15



In contrast, *Yamomoto* teaches that the TA should be limited to 150 ns to 500 ns in order to secure a proper sustaining pulse margin $(V_{SP})max - (V_{SP})min$ where V_{SP} is the minimum voltage necessary to keep the sustain pulse discharge and the V_{SP} max is a maximum voltage which can be applied to the panel in which non-accessed cells will not cause erroneous discharge. (Col. 3, lns. 20–31; Col. 1, lns. 15–23). The sustain pulse margin is necessary due to the inductance in the electrodes and/or interelectrode capacitance. (Col. 1, lns. 15–23). The choice of the setup pulse of the present invention, however, is not directed to solving a problem of inductance in the electrodes and/or interelectrode capacitance.

Thus, the values disclosed in the *Yamamoto* reference reflects the reference's concern regarding the sustain pulses' decreasing margin because the overall rising angle of the waveform in sustain pulses are affected by the inductance and capacitance of the electrodes. (Col. 1, lns. 5 – 22). The rising angle of the setup pulse waveform also exerts an influence upon the amount of wall charges that accumulate. However, the overall rising angle of the setup pulse waveform is not affected by the inductance capacitance of the electrodes since the rising angle is determined by the average voltage change rate. Thus, the problems encountered by *Yamamoto* and the considerations set forth by *Yamamoto* regarding a sustain pulse are not applicable to the setup pulse of the present invention.

With respect to Claims 100-107, *Yamamoto* does not teach the feature of using a two display electrodes and a data electrode for a total of three electrodes within each discharge cell. The Figures and values taught in *Yamamoto* relate to a vertical discharge type DC PDP which does not use the three electrode configuration of the present invention.

In contrast, as seen in Figure 1, the present invention includes scan electrodes 19a and sustain electrodes 19b formed on front substrate 11 and data electrodes 14 formed on back substrate 12. As seen in Attachment A, a surface discharge occurs between the scan electrodes 19a and the sustain electrodes 19b during the sustain period in the present invention.

With respect to Claims 108-115, *Yamamoto* further does not disclose a feature of a dielectric layer covering the display electrodes. The Figures and values taught in *Yamamoto* relate to a vertical discharge type DC PDP which does not have a dielectric layer covering the display electrodes.

In contrast, the present invention includes a dielectric layer 17, such as lead glass, which covers the scan electrodes 19a and sustain electrodes 19b. (Fig. 1)

Dependent Claims 52–57, 59–64, 66–71, 73–79, 83–87, and 89–99 depend from and further define Claims 51, 58, 65, 72, 82, and 88 and are thus allowable, too.

It is believed the present application is now allowable and an early notice of the same is requested.

If there are any questions with regards to this matter, the undersigned attorney can be contacted at the listed phone number.

Very truly yours,

SNELL & WILMER L.L.P.

Joseph W. Price
Registration No. 25,124
600 Anton Boulevard, Suite 1400
Costa Mesa, California 92626-7689
Telephone: (714) 427-7420
Facsimile: (714) 427-7799

◆ Schematic View of Functions of Respective Periods (Pulses) of Driving Waveform and Wall Charge Movement